What is claimed is:

1. A method of processing an output signal of an image sensor pixel in readout circuitry having a first capacitor element coupled to a second capacitor element, comprising the steps of:

   a. applying a reference voltage V_{REF} to the first and the second capacitor elements;

   b. applying a first sample signal V_{S1} from the image sensor pixel to the first capacitor element placing a charge on the first capacitor element;

   c. transferring the charge from the first capacitor element to the second capacitor element;

   d. applying a second sample signal V_{S2} from the image sensor pixel to the first capacitor element placing a charge on the first capacitor element; and

   e. transferring the charge from the second capacitor element to the first capacitor element so as to provide an output signal that is a function of the difference between the second sample signal V_{S2} and the first sample signal V_{S1}.

2. A method as claimed in claim 1 wherein step e. comprises transferring the charge from the second capacitor element to the first capacitor element so as to provide an output signal V_O where $V_O = V_{S2} - V_{S1} + V_{REF}$.

3. A method as claimed in claim 1 wherein V_{S1} is a sample voltage proportional to light intensity on the pixel and V_{S2} is a pixel reset voltage.

4. A method of processing an output signal of an image sensor pixel in readout circuitry having an operational amplifier with an input terminal, a reference terminal and an output terminal, a first capacitor element having first and second terminals with the second terminal coupled to the input terminal and a second capacitor element having first and second terminals with the second terminal coupled to the input terminal, comprising the steps of:

a. connecting the operational amplifier reference terminal to a reference voltage V_{REF};

b. applying the reference voltage V_{REF} to the first terminals of the first and the second capacitor elements;

c. applying a first sample signal V_{S1} from the image sensor pixel to the first terminal of the first capacitor element placing a charge on the first capacitor element;

d. transferring the charge from the first capacitor element to the second capacitor element;

e. applying a second sample signal V_{S2} from the image sensor pixel to the first terminal of the first capacitor element placing a charge on the first capacitor element; and

f. transferring the charge from the second capacitor element to the first capacitor element so as to provide an output signal V_O on the operational amplifier output terminal that is a function of the difference between the second sample signal V_{S2} and the first sample signal V_{S1}.

5. A method as claimed in claim 4 wherein $V_O = V_{S2} - V_{S1} + V_{REF}$.

6. A method as claimed in claim 4 wherein V_{S1} is a sample voltage proportional to light intensity on the pixel and V_{S2} is a pixel reset voltage.

7. A method of processing an output signal of an image sensor pixel in readout circuitry having an operational amplifier with an input terminal, a reference terminal connected to a first reference voltage and an output terminal, a first capacitor element having first and second terminals with the second terminal coupled to the input terminal, a second capacitor element having first and second terminals with the second terminal coupled to the input terminal, first switch means adapted to be connected between a second reference voltage and the first capacitor element first terminal, second switch means adapted to be connected

between a pixel and the first capacitor element first terminal, third switch means adapted to be connected between a third reference voltage and the second capacitor element first terminal; fourth switch means connected between the operational amplifier input terminal and the output terminal; fifth switch means connected between the second capacitor element second terminal and the operational amplifier output terminal; and sixth switch means connected between the first capacitor element first terminal and the operational amplifier output terminal, comprising the steps of:

a. opening all of the switch means;

b. closing the first, third and fourth switch means;

c. opening all of the switch means;

d. closing the second and fifth switch means;

e. opening the fifth switch means and closing the fourth switch means;

f. opening all of the switch means;

g. closing the third and sixth switch means;

h. reading the output voltage Vo on the operational amplifier output terminal.

8. A method as claimed in claim 7 wherein the first, second and third reference voltages are equal to V_{REF}.

9. A method as claimed in claim 8 wherein step d. includes applying a pixel sample signal V_{S1} to the first capacitor element.

10. A method as claimed in claim 9 wherein step e. includes applying a pixel sample signal V_{S2} to the first capacitor element.

11. A method as claimed in claim 10 wherein $V_O = V_{S2} - V_{S1} + V_{REF}$.

12. A method as claimed in claim 11 wherein V_{S1} is a sample voltage proportional to light intensity on the pixel and V_{S2} is a pixel reset voltage.

13. Readout circuitry for image sensor pixels comprising:

- first capacitor means having first and a second terminals;
- second capacitor means having first and a second terminals;
- amplifier means having an input terminal and an output terminal, wherein the second terminals of the first and second capacitor means are connected to the amplifier means input terminal;
- first switch means connected to the first capacitor means first terminal;
- second switch means connected to the second capacitor means first terminal;
- third switch means connected between the amplifier means input terminal and output terminal;
- fourth switch means connected between the second capacitor means second terminal and the amplifier means output terminal; and
- fifth switch means connected between the first capacitor means first terminal and the amplifier means output terminal.

14. Readout circuitry as claimed in claim 13 wherein the amplifier means further includes a reference terminal adapted to be connected to a reference voltage V_{REF}.

15. Readout circuitry as claimed in claim 14 wherein the first switch means comprises:

- first coupling means adapted to couple the first capacitor first terminal to a reference voltage V_{REF}; and

- second coupling means adapted to couple the first capacitor first terminal to a pixel.

16. Readout circuitry as claimed in claim 15 wherein the second switch means is adapted to couple the second capacitor means first terminal to a reference voltage V_{REF}.

17. Readout circuitry as claimed in claim 16 comprising means for controlling the first and second coupling means and the second, third, fourth and fifth switch means.

18. Readout circuitry as claimed in claim 17 wherein the control means is adapted to close the second switch means, the third switch means and the first coupling means substantially simultaneously.

19. Readout circuitry as claimed in claim 18 wherein the control means is adapted to close the fourth switch means and the second coupling means substantially simultaneously.

20. Readout circuitry as claimed in claim 19 wherein the control means is adapted to close the third switch means and the second coupling means substantially simultaneously.

21. Readout circuitry as claimed in claim 20 wherein the control means is adapted to close the second switch means and the fifth switch means substantially simultaneously.

22. Readout circuitry as claimed in claim 16 wherein the first and second coupling means and the second, third, fourth and fifth switch means are transistors.

23. Readout circuitry as claimed in claim 16 the first and second coupling means and the second, third, fourth and fifth switch means are CMOS transistors.